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DOCKET NUMBER: 209665US2/cp

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:
Seiichi MORI

: GROUP: 2811

SERIAL NUMBER: 09/876,019

: ATTENTION:
Application Division
Customer Corrections

FILED: JUNE 8, 2001

FOR: SEMICONDUCTOR MEMORY INTEGRATED CIRCUIT AND ITS
MANUFACTURING METHOD

REQUEST FOR CORRECTED OFFICIAL FILING RECEIPT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The Patent Office is requested to provide a corrected Official Filing Receipt for the attached. If you have any questions, please do not hesitate to contact us.

No fees are required. However, in the event that a fee is required, please charge the appropriate amount to our Deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

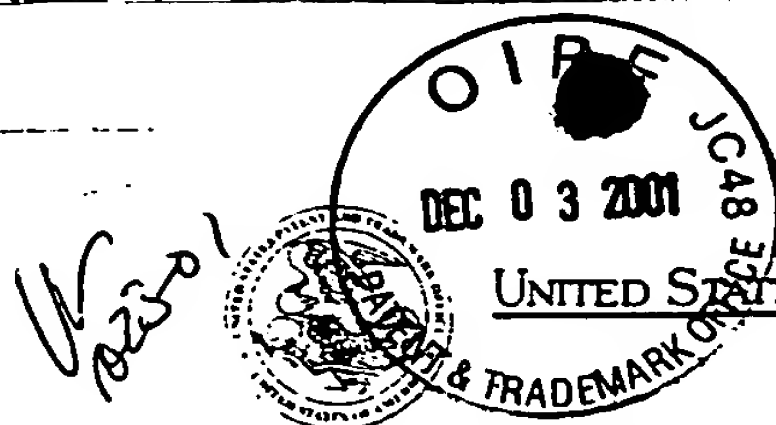
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APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
09/876,019	06/08/2001	2811	1080	209665US-2	36	20	6

CONFIRMATION NO. 7457

22850
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UPDATED FILING RECEIPT



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Date Mailed: 10/17/2001

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

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Assignment For Published Patent Application

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Domestic Priority data as claimed by applicant

Foreign Applications

JAPAN 2000-174127 06/09/2000
JAPAN 2001-171612 06/06/2000

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Projected Publication Date: 01/24/2002

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Early Publication Request: No

Title

Semiconductor memory integrated circuit and its manufacturing method

Preliminary Class

257

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MAIER & NEUSTADT, P.C.

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DRAWINGS: 41

PLEASE NOTE THAT THE FOREIGN APPLICATIONS INFORMATION IS INCORRECT.
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JAPAN 2000-174127 06/09/2000
JAPAN 2001-171612 06/06/2001